Maximizing ROI for 7-nm SoCs with Synopsys' Convergent Digital Design Platform

Synopsys

ABSTRACT

Scaling to lower geometries is constrained not only by metallurgy and lithography challenges, but also by the need for an evolution in physical design methodologies to extract the maximum ROI at the 7-nm process node. With the advent of cell height reduction for pitch scaling, heterogeneous stack-driven RC management, and the ever-increasing impact of waveform distortion as well as non-Gaussian effects, this node demands a flow-wide reassessment for best ROI. In this talk, Synopsys' senior R&D member will describe how several key innovations in IC Compiler II, along with a distinctively architected integration flow with Design Compiler, StarRC and PrimeTime, offers the most compelling solution for designers to realize their 7-nm entitlement. Data will be presented to show that this flow is reducing design-in-margins, while offering higher utilization rates, best QoR and the fastest path to design closure.

SYNOPSYS®
Silicon to Software™

Maximizing ROI for 7-nm SoCs with Synopsys' Convergent Digital Design Platform

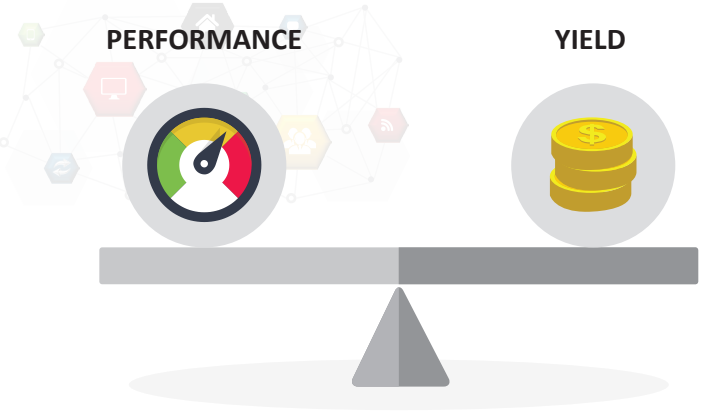
Deploying Platform-Wide Innovations to Deliver Optimal Design QoR

Dr. Henry Sheng, R&D Group Director, Design Group, Synopsys

September 2017

N7: For SoCs Everywhere

Optimal Power, Performance and Area with Joint Reference Flow



PROCESS + REFERENCE FLOW + IMPLEMENTATION

SYNOPSYS®

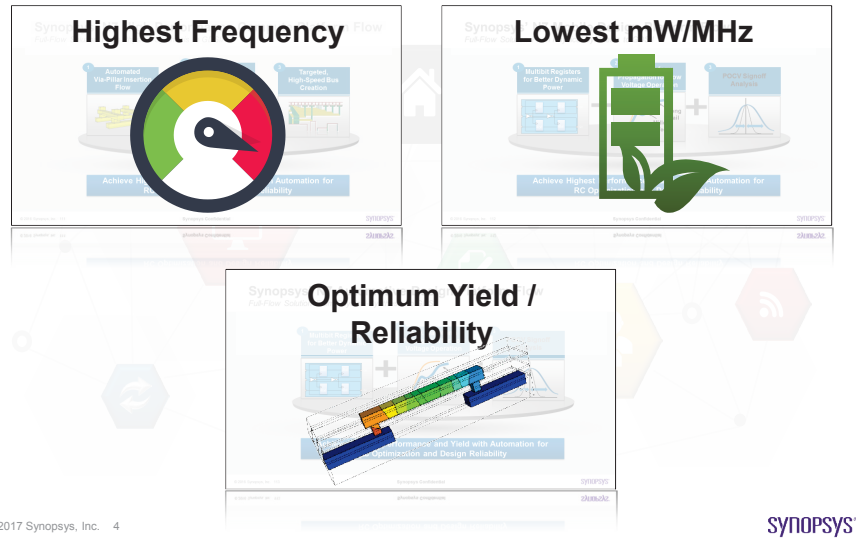
Differentiated Segments, Differentiated Solutions

Collaborative Enablement Accelerates Design Bring-up

SYNOPSYS®

Synopsys: Maximizing Design Entitlement

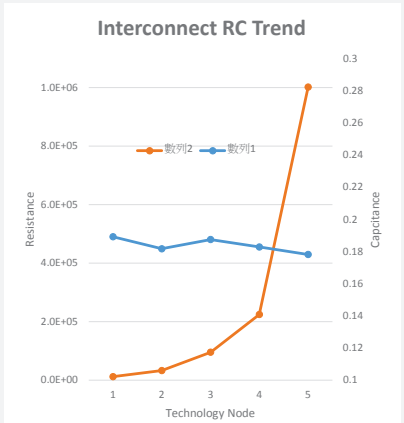
Delivering Design Differentiation and Expanded ROI

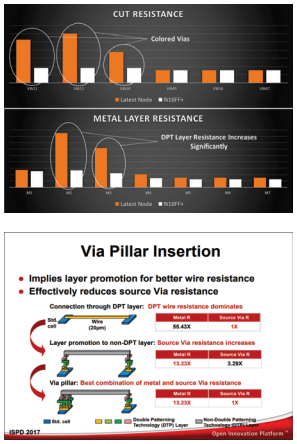


SYNOPSYS®

HPC: Interconnect as The Primary Challenge

Increased Resistivity Impacts Overall Design Performance





Interface-Layer Effects and Grain Scattering Impacting Resistance Scaling

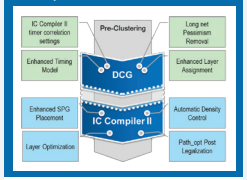
Source: Serkan Kincal, et al., "RC Performance Evaluation of Interconnect Architecture Options Beyond the 10-nm Logic Node," IEEE (2014)

Source: "Physical Design Challenges and Innovations to Meet Power, Speed, and Area Scaling Trend," LC LU, TSMC Fellow/Senior Director, R&D, ISPD 2017

Performance-Driven Pre-Route Technologies

Algorithmic Enhancements in IC Compiler II Drive Optimal QoR

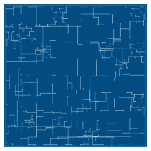
ENHANCED DCG / IC COMPILER II SPG FLOW
Tighter Correlation, Improved OOTB Result



FREQUENCY UPLIFT

percent

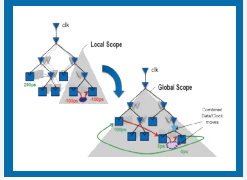
ADVANCED HIGH-FANOUT-NET SYNTHESIS
Enhanced Buffer Count and Wire Topologies



LOWER WIRELENGTH

percent

GLOBAL ANALYTICAL CLOCK-AND-DATA OPTIMIZATION
Higher Performance, Area and Leakage Benefits



FREQUENCY UPLIFT

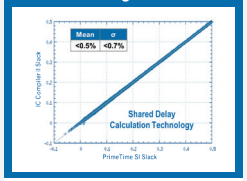
percent

Wiring and Topology Optimization Maximizes Achievable QoR

Performance-Driven Post-Route Technologies

Innovating Throughout Implementation to Maximize Signoff Correlation

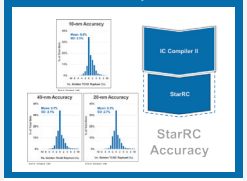
PRIMETIME DELAY CALCULATOR INSIDE IC COMPILER II
Tighter Signoff Correlation, Enables Margin Reduction



PT-SI CORRELATION

percent

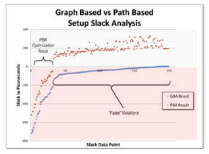
IN-DESIGN STARRC EXTRACTION
Full Signoff Accuracy Available for Optimization



STARRC CORRELATION

Signoff accuracy

PATH-BASED POST-ROUTE OPTIMIZATION
Prevents Over-Design During Closure



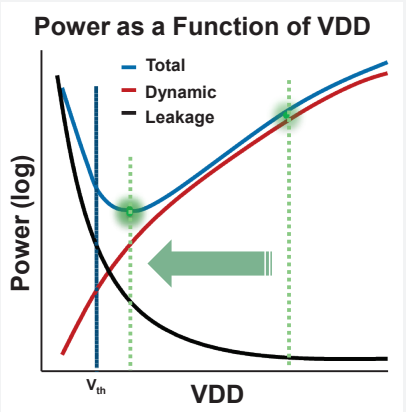
LEAKAGE REDUCTION

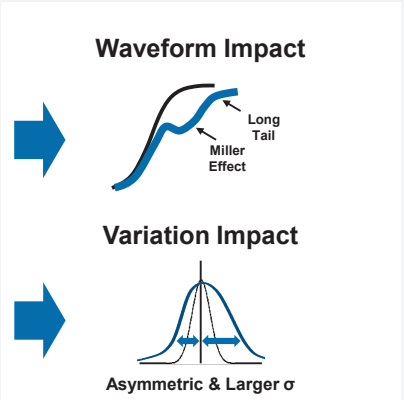
percent

Convergent Signoff Closure Within The Implementation Flow

Mobile: Lower Voltages Bring New Challenges

Significant Power Reduction Demands Flow-Wide Enhancements



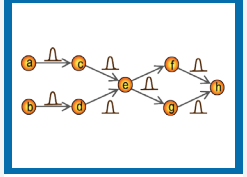


Small Form-Factors and Battery Life Demand Innovations in Correlation, Power Reduction and Area Minimization

Area and Power Focused Technologies

Minimizing Design Margins, Minimizing Structural Variation

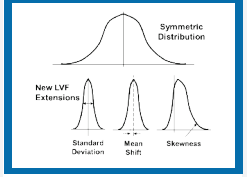
PARAMETRIC OCV (POCV) THROUGHOUT THE FLOW
Reduced Margins, Lower Leakage



AREA

percent

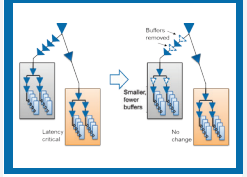
MOMENT-BASED POCV DESIGN OPTIMIZATION
Enhanced Accuracy for Low Voltage Operation



PT-SI CORRELATION

percent

GLOBAL CONTEXT-AWARE CLOCK SYNTHESIS
Smaller Clock Trees, Fewer Buffers, Lower Area



POWER REDUCTION

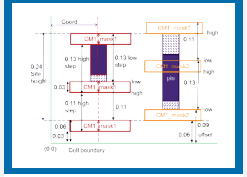
percent

Signoff Correlation is Key in Reducing Over-Design

Area and Power Focused Technologies

Innovating To Maximize Process ROI

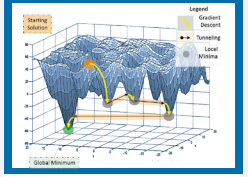
ENHANCED CUT-METAL ROUTING FLOW
Reduced Line-End Capacitance, Lower Power



POWER REDUCTION

percent

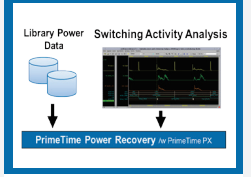
SOLVER-BASED TOTAL-POWER OPTIMIZATION
Lower Leakage and Dynamic Power



POWER REDUCTION

percent

ACTIVITY-BASED POWER ANALYSIS AND OPTIMIZATION
Attacks Leakage and Dynamic Power



POWER REDUCTION

percent

Broad Optimization Technologies Deliver Highest Power Benefits

Automotive: Maximize Reliability and Yield

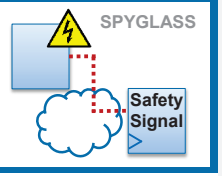
Delivering Highest Performance Under Most Challenging Conditions

SMARTPHONE		AUTOMOTIVE
28 nm → 7 nm	Process	>180 nm → 7 nm
100M+	Design Sizes (µP/C)	1M to 100M+
>2GHz	Frequencies	~100MHz to >2GHz (+ TFLOPs of GPU Data)
0.5V to 1.8V	Voltages	~1V to >60V
0 to 40 °C	Temperatures	-40 to 85/155 °C
1-3 years	Lifetime	~15 years
<2%	Failure Rates	Target Zero Failure

Reliability Focused Technologies

Target Known Failure Mechanisms To Enhance Device Longevity

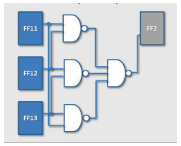
SOFT-ERROR DESIGN ANALYSIS
Targeted Analysis to Drive Optimization



SPFM

ISO26262
certified

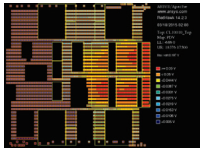
ERROR-TOLERANT CELL-AWARE OPTIMIZATION
Broadly Maximizes Fault Tolerance



INSERTION RATE

100
percent

ANSYS REDHAWK IN-DESIGN ANALYSIS
Highest Accuracy Signoff Solution



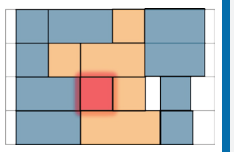
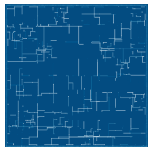
IN-DESIGN OPTIMIZATION

Signoff
accuracy

Delivering Maximum Productivity for Automotive Grade Designs

Yield-Aware Performance Technologies

Manufacturability as a Key Optimization Objective

LDE-AWARE CELL LEGALIZATION AND OPTIMIZATION *Maximizes Utilization and Performance*	DESIGN-WIDE WIRE-LENGTH REDUCTION *Yield Maximization*	DFM-AWARE WIRING AND METAL OPTIMIZATION *Seamless, In-Flow Wire/Via Optimization*
		
UTILIZATION RATE	LOWER WIRELENGTH	INSERTION RATE
percent	percent	percent

Enhances Manufacturability for Increased ROI

SYNOPSYS

Expanding Platform Challenges at 7 nm

Emerging Nodes Bring a Host of Challenges. Collaboration Brings Maximum Node Entitlement

- **Emerging nodes have innate complexity and targeted flows put even greater demands on EDA**
  - Growing design sizes, more modes/corners
  - Need for coordinated treatment of effects across full tool chain
  - Increased need for productivity enhancements
- **Close ecosystem and designer collaboration is key in maximizing what can be achieved at each node**
- **Synopsys is at the forefront of enabling the highest ROI at this exciting node**

SYNOPSYS

SYNOPSYS®
Silicon to Software™

Thank You

SYNOPSYS®
Silicon to Software™